Patent

#14

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Vora

Art Unit: 2512

Examiner: Sara Crane

Serial No. 08/654,760

Filed: 5/29/96

For: VERTICALLY INTEGRATED FLASH EEPROM FOR GREATER DENSITY AND LOWER COST

Box AF
Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Morgan Hill, California
August 3, 1998

APPEAL BRIEF

Dear Sir:

In response to the final rejection mailed 3/10/98 and the Notice of Appeal mailed June 9, 1998, please find below the Appeal Brief for the above identified case as follows.

Real Party In Interest

The real party in interest in the above entitled patent application is the inventor Madhukar Vora there being no assignee

Related Appeals & Interferences

There are no other related appeals or interferences.

Status of the Claims

There are currently five claim pending in this case. In the final rejection dated 3/10/98, former Examiner Giordana imposed some rejections under 35 U.S.C. §112,

Para. 2 for indefiniteness. In response to this rejection, the undersigned filed an amendment which made some amendments to the claims to fix those indefiniteness problems and made some additonal amendments to try and put the claims in better condition for appeal. The undersigned also submitted an declaration of Madhu Vora under Rule 132 with a detailed comparison of the structure of the prior art Mori reference to the claimed structure to show the significant differences in EEPROM memory array density that result from the differences in structure between the Mori cell and the Vora cell. I had a telephone interview with new Examiner Sara Crane. In that interview, I explained the differences in structure and how previous Examiner Giordana had misinterpreted the claims as amended in response to her first office action and had misinterpreted the teachings of the Mori reference. I explained how these two error had removed the very foundations of the prima facie case of obviousness and why the final rejection should be withdrawn, but Examiner Crane remained unmoved. I had the amendment after final and the Rule 132 Declaration hand carried to Examiner Crane and called her to follow up, but she said she had not received it or not received all of it. I had both the Amendment and the Rule 132 Declaration handcarried to Examiner Crane again after she said she did not have it and I asked her to please notify me before the end of July whether she was going to maintain the final rejection and to notify me of the status of the claims, but she did not do so. I called her twice and she did not return my calls. I finally reached her prior to writing this appeal brief to inquire as to the status of the claims, and she said the clerks had the amendment after final, but she said she was going to maintain the final rejection originally imposed by Examiner Crane and was not going to enter any of the amendments from the amendment after final. It is unclear to me whether at that time she had actually read the amendment and remarks and the Rule 132

Declaration. I have received no formal notifications of status of these claims from the PTO so I do not know if the amendments in response to the indefiniteness rejections were or were not entered. However, it appears that the claims given below are still finally rejected. The claims given below are the claims as they existed after the first Office Action and my response thereto and do not include any amendments from the amendment after final. I believe these claims to be the claims on appeal. Perhaps Examiner Crane in her response will notify the Board of any amendments from the amendment after final that were actually entered.

All five of the following claims are on final rejection and are appealed.

1. (Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by alternating N-type and P-type doped layers in said substrate [intersecting] and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layer surround said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from and overlying said alternating N-type and P-type [materials] layers by a layer of gate insulating material;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said [flaotign] floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS

transistor formed in said substrate.

2. (Amended) A nonvolatile memory cell array comprised of a plurality of nonvolatile memory cells, each memory cell comprising:

a semiconductor substrate having a drain region of a first conductivity type formed therein and having a surface coincident suitable to act as a drain region of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel [region] of a vertical MOS transistor formed in said substrate;

a [first] source region of said semiconductor substrate [between said buried layer and said surface of said substrate, and a second region of said semiconductor substrate] below said channel region [buried layer, both said first and second regions] source region being doped so as to have [a] said first conductivity type;

[a first layer of insulating material covering said surface of said substrate;]

a recessed gate window in the form of a well etched in said semiconductor substrate through said first layer of insulating material, said well being deep enough to penetrate through said [buried layer] channel region and into said source region such that at least some portion of the side wall or sidewalls of said trench are bordered by said source, drain and channel regions [recessed gate window intersect said buried layer and said first and second regions of said semiconductor substrate];

[a second] an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well; [with]

an insulating layer formed over said self aligned floating gate [conductive material] so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said [intersection of said well with said buried layer] channel region;

a word line comprising conductive material deposited [on said first insulating layer] so as to extend into said well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed [over] so as to insulate at least a portion of said word line; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated from said word line by said second layer of insulating material[, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transitor].

Please add a new claim 3 as follows:

3. A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by a first layer of N-type conductivity and having a surface coincident with the surface of said substrate and forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said

substrate and adjacent to and underlying said first layer relative to the surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying said first, second and third layers and insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed on the surface of said substrate so as to be in electrical contact with the surface of said first layer coincident with the surface of said substrate at each cell in said array, and

a spacer layer of insulating material insulating said word line contact from said bit line contact.

Please add a new claim 4 as follows:

4. The apparatus of claim 3 wherein said bit line contact contacts said first layer at all points between said spacer layers of the word line contacts of adjacent memory cells.

Please add a new claim 5 as follows:

5. The apparatus of claim 3 wherein said bit line contact contacts said first layer at at

least some points between said spacer layers of the word line contacts of adjacent memory cells and runs over the top of said word line and is insulated therefrom by said spacer layer.

Status of Amendment After Final

For the reasons given above and for lack of any formal communication from the PTO in response to the amendment after final, the undersigned does not know the exact status of the amendment after final.

Summary of the Invention

The invention of the claims on appeal (hereafter the Vora cell) is a vertically integrated EEPROM cell which has two features which distinguish it over the prior art Mori reference. These two structural differences make an array of Vora cells about 3 to 4 times as dense as an array of vertically integrated EEPROM cells constructed in accordance with the teachings of Mori.

The first of the two principal structural differences that distinguish the Vora cell is the use of a self aligned vertical floating gate. This self aligned gate is shown at 22 and 22' (it is actually circular or has the same shape as the well in the cross section through the final Vora cell shown in Figure 5. The key thing about this self aligned floating gate is that it is made without using a mask by depositing doped poly layer 102 in Figure 20B (see page 9, lines 28-30 and step 33 of the process flow table starting on page 13) over the entire substrate so that it goes down into the wells of all the EEPROM devices. The self aligned floating gates are then formed without using a mask by performing an anisotropic etch to etch back all the horizontal portions of the doped poly layer 102 so as to leave only the vertical portions. This is taught in the specification at page 9, line 33 to page 10, line 3 and at step 34 of the table starting on page 13, as quoted below:

> Next, a layer of P type doped polysilicon 102 is deposited over the complete structure from which the floating gate 22 in Figure 5 will be formed to leave the structure as shown in Figures 20A, B and C.

> Typically, about 1000 angstroms of polysilicon is deposited and is doped P type with chemical dope of phosphorous either during or after deposition to a resistivity of 50 ohms per square.
>
> To form the floating gate, the doped polysilicon is etched back off all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure shown in Figure 5.

This leaves the structure as shown in Figure 21B. The fact that no mask is used to form the floating gate causes the size and spacing of all the components of the vertically floating gate to be tighter packed since there are no alignment tolerances required by design rules to align the floating gate to other previously formed structures and there are no alignment tolerances to align other subsequently formed structures to the floating gate. This means that the Vora cell is much smaller than the prior art for this reason alone. The reasons the Vora cell is much smaller can be understood by reference to the Vora Rule 132 Declaration and the accompanying drawings and design rules Mr. Vora included therewith. The small size of the Vora cell is the key to it becoming economically viable to replace hard disk drives or other nonvolatile memory for storing programs in some battery driven applications, especially portable computers and hand held wireless devices.

The second principal difference over the Mori prior art of the Vora cell is that the bit line (30 in Figure 5) is formed <u>on top of the substrate</u> and not in the substrate and makes contact with the drain (14 in Figure 5) of <u>every</u> cell <u>at the location of the cell</u>. The pertinent portion of the specification, from page 5, lines 9 et seq. is quoted below:

> Figure 5 shows in vertical section the completed device. To reach the state of construction shown in Figure 5, a layer of oxide 29 is grown on the second polysilicon layer 28. Then a mask is formed over the second polysilicon layer 28 to protect the portion thereof overlying the well which it fills. Thereafter, an anisotropic etch is performed to etch down through the polysilicon layer 28, the ONO layer 24, the oxide layer 16

and part of the way through the N-type silicon layer 14 to open a contact well for the bit line 30.

After this contact well is opened, an annular oxide spacer, sections of which are shown at 32 and 32', is formed to seal and insulate the sides of the structure from the bit line to be formed next. The oxide spacer is formed by growing or depositing a layer of oxide over the entire structure and anisotropically etching it back to leave the vertical sections of oxide.

The bit line is shared by all devices in a row and is formed by depositing a third layer of polysilicon 30 over the entire structure and etching it to selectively make contact with the N-type silicon layer 14 which forms the drain of the vertical annulus MOS transistor formed inside the well. **The source of the vertical MOS transistor is the N-type substrate 10.** The channel region for this transistor is formed by the P-type silicon layer 12. The gate oxide between the channel region and the floating gate 22 is oxide layer 20. The control gate is comprised of second polysilicon layer 28, and extends down into the page and up out of the page to form the word line.

The section of the specification in bold also teaches another difference which is significant to the issue of size. In the Mori reference, each row of cells has a buried isolation structure isolating it from its neighboring rows (shown at 15 in Figure 1). This buried isolation region eats up a lot of chip real estate. No such isolation structure is needed in the Vora cell because every cell shares a common source region which is the N-type substrate 10.

Issues For Review By the Board

1. Whether the prima facie case of obviousness or anticipation was ever correctly established by Examiner Giordana and maintained by Examiner Crane in support of the final rejection given their misinterpretation of the amended claims and misreading of the teachings of Mori.

2. Even if the prima facie case is deemed by the Board to have been correctly established, whether the new evidence submitted by Mr. Vora overcomes the prima facie rejection.

Grouping of Claims

All of the independent claims 1, 2 and 3 contain limitations that the floating gate be self aligned and that the bit line be formed on or over the substrates so as to make contact with the drain of the cell, so all claims are grouped together with patentability hinging at least on these two features, or either standing alone.

Argument

The Indefiniteness Rejections

Examiner Giordana rejected claim 2, line 4 as indefinite as it is unclear with the "surface" is coincident. Claim 2 as it stood before the final rejection and as quoted above had a typographical error in it. The undersigned tried to correct this typographical error in the amendment after final by amending the affected clause as follows:

> a semiconductor substrate having a top surface and having a drain region of a first conductivity type formed [therein and having a] below said top surface so as to have a surface coincident with said top surface of said substrate and suitable to act as a drain region of a vertical MOS transistor;

It is unclear whether Examiner Crane has allowed this amendment to be entered under Rule 116. If she has, then the indefiniteness rejection should be moot. The amendment does not go to the merits of the claim and only clarifies where the drain region top surface lies relative to the top surface of the substrate. If this amendment is allowed, the indefiniteness rejection is moot. If it has not been allowed, the undersigned is willing to cancel the claim.

Another indefiniteness rejection was imposed on claim 2, line 4 based upon the same typographical error in that Examiner Giordana could not understand how a surface which is a two dimensional entity could act as a drain region which is a three

dimensional entity. If the above quoted amendment has been allowed to be entered by Examiner Crane, this rejection should be rendered moot. If she has refused to enter this amendment for some reason, the undersigned is willing to cancel the claim, although it would seem a recommendation by the Board to simply make the above quoted amendment would be more just than forcing the claim to be cancelled.

Claim 3 was rejected for indefiniteness for lack of antecedant basis for the phrases "word line contact" and "bit line contact" in lines 22 and 23. The undersigned has attempted to correct this error by making the following amendment in the amendment after final:

> a spacer layer of insulating material insulating said word line [contact] from said bit line[contact].

It is unclear whether Examiner Crane has allowed this amendment to be entered under Rule 116. If she has, then the indefiniteness rejection should be moot. The amendment does not go to the merits of the claim, and it would seem that justice would be better served to allow this amendment to be made either after final or upon recommendation of the board.

As to claims 2 and 3, the undersigned believes that the notice function of these claims has been served in light of the specification and drawings and those skilled in the art would understand perfectly well what was meant by the language even if it was slightly flawed. It would be gross miscarriage of justice to force the applicant to cancel 4 claims simply because these minor amendments, which do not raise new issues or require a new search, were not allowed after final rejection.

THE PRIMA FACIE CASE OF OBVIOUSNESS HAS NOT BEEN PROPERLY ESTABLISHED BECAUSE THE CLAIM LANGUAGE HAS NOT BEEN PROPERLY CONSTRUED AND GIVEN PROPER WEIGHT

The "Self Aligned" Limitations in Claims 1, 2 and 3 and the dependent claims 4 and 5 Defining The Structure of the Floating Gate Has Not Been Construed Properly And Has Been Improperly Generalized

Claim 1 contains the following limitations defining the structure of the floating gate:

> said well having a floating gate of conductive material formed therein

which is self aligned to not extend laterally beyond edges of said well

Claim 2 contains the following limitations defining the structure of the floating gate:

> a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well

Claim 3 contains the following limitation regarding the structure of the floating gate:

> said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well

The Examiners seems to have construed this "self aligned" limitation in each independent claim in the final rejection as meaning solely that the floating gate material does not extend beyond the edges of the well. That is not actually what the limitation means in light of the teachings in the specification and drawings and the process flow table regarding how the floating gate is formed. The Board should also take judicial notice of the fact that people skilled in the art understand the term "self aligned" in integrated structures to mean "formed without using a mask", so even if the Examiners had not actually read the specification, the term "self aligned" should have conveyed a different meaning than solely that the floating gate material did not extend past the edges of the well. While it is true that the Vora cell floating gate does not have any poly extending beyond the edges of the well, the term self aligned is intended to convey structural relationships, i.e., distances, between the other elements of the cell and the floating gate which are smaller because the floating gate is stated to be self aligned, i.e. was formed without using a mask.

The specification teaches that the self alignment of the floating gate is achieved in steps 33 and 34 of the process detailed in the table beginning at page 13. In step 33, the poly layer 102 is deposited, and, in step 34, the poly layer 102 is etched back *to remove all poly from horizontal surfaces.* This leaves the floating gate material deposited only on the vertical surfaces of the well or trench. The specification teaches:

> Next, a layer of P type doped polysilicon 102 is deposited over the complete structure from which the floating gate 22 in Figure 5 will be formed to leave the structure as shown in Figures 20A, B and C. Typically, about 1000 angstroms of polysilicon is deposited and is doped

> P type with chemical dope of phosphorous either during or after deposition to a resistivity of 50 ohms per square.
>
> To form the floating gate, the doped polysilicon is etched back off all horizontal surfaces and part way down into the recessed gate windows 88 and 90 to leave the segments of polysilicon shown at 102 in Figure 21B. These segments of doped polysilicon 102 correspond to the floating gate 22 in the finished structure shown in Figure 5.

The drawings clearly show a self aligned floating gate which has no horizontal components either on the bottom of the well or overlying the gate oxide and top surface of the substrate at the top of the well.

These passages from the specification plus the drawings clearly teach that a self aligned floating gate, as that phrase is used in the claims is intended to convey a meaning of a floating gate inside the well but having conductive material only on the vertical sidewalls of the well with no conductive material on the bottom of the well or overlying any portion of the top surface of the substrate and having distances which are closer to other structures in the cell than is possible in the Mori cell where a mask is used to define the floating gate.

To be more precise about exactly what distances are closer in the Vora cell please refer to the Vora Rule 132 declaration and its drawings. Mr. Vora points out these smaller relative distances in his declaration as follows:

> In contrast, none of these alignment tolerances defined by POLY 2-4 + POLY 2-3 or POLY 1-4 is needed in the Vora cell because a mask is not used to form the floating gate in the Vora cell. Basically, in the Vora cell, a poly 0 layer is laid down after formation of the trenches, and then etched back to remove all horizontal components of poly 0 from the bottom of the trenches and any horizontal components at the top of the trenches. Because no mask is used for this, no alignment tolerances or wasted space is necessary in the Vora cell.

The minimum distances between adjacent structures which must exist and the definition of what structures are referred to by the Poly 2-4 and Poly 2-3 and Poly 1-4 design rules is given at page 2 of Exhibit A to the Vora declaration. A graphical illustration of the actual distances defined by these design rules which are required in the Mori cell

(because he teaches use of a mask to form his floating gate) is given at page 3 of Exhibit A to the Vora Rule 132 Declaration where an actual layout of the Mori prior art cell using these design rules is shown in plan view.

Examiner Crane apparently could not understand the drawing shown at page 3 of Exhibit A showing the Mori cell as she did not consider this to be significant and maintained the final rejection. In an attempt to clarify the exact significance of the meaning of a self aligned floating gate, I have attached as Exhibit 1 to this brief Mr. Vora's layout of the Mori cell and have added reference letters and numbers to it that correspond to the Mori patent drawing Figure 1a to show the various structures comprising the cell. I have also added reference numbers to the various dimension indicators the distances of which are controlled by the design rules to clarify exactly which distances between exactly which structures are required in the Mori cell because he uses a mask to define his floating gate whereas the Vora cell does not.

There is no doubt that Mori uses a mask to form his floating gate and does not use a self aligned process. If Mori taught the same invention as the applicant, there would be no horizontal component of the Mori floating gate (FG in Figure 1a) either at the bottom of the well or above the gate oxide (note how the Mori floating gate rises to the top of the well and makes a right angle turn).

Mori specifically teaches that the floating gate is formed by depositing first poly and then masking and etching to define the floating gates in each trench. At Mori, Col. 9 in the section entitled "2.3. Gate Conductor Formation", at lines 23 through 29, Mori teaches:

> "The poly 1 deposition forms a conductive layer within each trench, including a vertically extending section 82. The vertically extending section 82 covers the gate oxide 74 on the sidewalls of the trench, leaving a central cavity 84 in the trench.
>
> The poly 1 layer is then **patterned** and etched to define the floating gates."

Those skilled in the art know that the process being referred to in the quoted passage is a process which uses a mask to "pattern", i.e., define the limits of the floating gate and is not a self aligned process. Self aligned processes do not use masks, and that is why they

are preferred over process steps using masks because in self aligned processed, there are no registration errors.

To understand the significance of the fact that Mori uses a mask and Vora does not, please refer to Exhibit 1 attached. The outline of the Mori floating gate is designated FG in Exhibit 1. The outline of the trench is shown at 22. The outline of the bit line is shown at 34. The outline of the word line is designated PG for program gate.

Because Mori uses a mask to define his floating gate and Vora does not, the distances or alignment tolerances designated A, B and C are not needed in the Vora cell whereas they are needed in the Mori cell. The distance A is the distance between the trench 22 and the edge of the word line. The minimum allowable spacing between the edge of the trench and the edge of the word line is defined by design rule POLY2-4 and is 0.5 microns in 1 micron design rules. The distance B is the distance between the edge of the word line PG and the edge of the floating gate poly. The minimum distance this can have in the Mori cell is defined by design rule POLY2-3 and is 0.5 microns in 1 micron design rules. The distance C is the distance between the edge of the floating gate and the edge of the bit line 34. The minimum distance this can be is defined by design rule POLY1-4 and is 0.5 microns in 1 micron design rules.

None of distances A, B or C is necessary in the Vora cell (see page 4 of Exhibit A to the Vora Rule 132 declaration - attached hereto as Exhibit 2) because of the use a self aligned floating gate. This is because the anisotropic etch that removes all horizontal components of the poly layer used to form the floating gate guarantees that there will be no poly portions of the floating gate extending up out of the trench because that would be a horizontal portion. This means that there is no need to guarantee a minimum space comprised of A + B between the edge of the trench and the edge of the floating gate portion lying on top of the substrate. This means adjacent cells along the same bit line can be closer together. Also, there is no need to gurantee a minimum space C between the edge of the portion of the floating gate lying on top of the substrate and the edge of the bit line. This means the bit lines can be narrower which means that the Vora cell columns can be packed closer together. Thus, the Vora cell is substantially smaller than the Mori cell and an array comprised of millions of Vora cells will be about 3-4 times as dense as an array of the Mori cells, i.e., for the same die size, there will be 3 to 4 times more Vora

cells than Mori cells.

Thus, in claims 1-5, the phrase self aligned floating gate structure should be interpreted by skilled artisans and the Federal Circuit as a floating gate with conductive material deposited only on the vertical surfaces of the well with no horizontal component on top of the substrate around the top edge of the well and no horizontal component at the bottom of the well and with narrower bit lines than the prior art and less distance across the cell along the long axis of the bit line, the combination of these smaller horizontal and veritcal dimensions for a single cell enabling tighter spacing between rows and columns of an array. This means a megabyte of Vora cells is a lot cheaper to make than a megabyte of Mori cells.

Claim limitations are to be interpreted in accordance with the language of the claims themselves, the specification and drawings and the prosecution history. Markman v. Westview Instruments, Inc., 34 USPQ2d 1321 (Fed. Cir. 1995). The United States Patent and Trademark Office has no license to interpret claims differently than the courts as the Federal Circuit pointed out in In re Donaldson, 29 USPQ2d 1845 (Fed. Cir. 1994). Claims terms are to be given their ordinary meanings unless the specification has given them special meaning. Intellicall Inc. v. Phonometrics Inc., 21 USPQ2d 1383 (Fed. Cir. 1992). Here, there is no ordinary meaning for the term self aligned in vertically integrated structures because the process of self alignment of floating gates in vertical transistors is relatively new and the term is not believed to yet have an established meaning to artisans. However, it should at least have some meaning to persons skilled in the art at least suggesting that no mask is used to make the floating gate. The term "self aligned" does have an established meaning in **planar** or horizontally constructed MOS structures. In planar MOS devices, a self aligned gate means that the edges of source and drain implants are aligned with the edges of spacer insulation layers formed at the edges of MOS gates by using the gate and spacers as an implant mask. In other words, there is no need for a mask that defines the inner edges of the source and drain implants because they are defined by the edges of the gate spacers. But in vertical structures, this meaning does not apply and there is no evidence that the undersigned is aware of or the inventor is aware of that indicates that self alignment of a floating gate in a vertically integrated MOS device has any established

meaning other than the meaning for the term which can be gleaned from the applicant's specification teaching use of an anisotropic etch with no mask to define the horizontal limits of the floating gate as limited to the extents of the trench. Title of the process flow schedule in the table on page 13 of the Vora application indicates that it is a method for making a self aligned EEPROM memory cell. A person skilled in the art, given all the teachings of the specification and drawings, would understand exactly what a self aligned floating gate was and the significance of that fact to the size of the cell as proved by the Rule 132 Declaration of Mr. Vora.

Accordingly, the meaning of the term "self aligned floating gate" in the claims should have been the meaning which can be gleaned from applicant's specification. The Examiner's did not do this. Instead, they both thought it meant that the floating gate could be formed with a mask so long as the floating gate material did not extend beyond the limits of the trench. This is impossible to do with a mask as anybody skilled in this art knows. They then proceeded to look at Figure 1a of Mori where the floating gate FG **appears** to not extend beyond the limits of the trench and imposed the final rejection. In doing this, they both ignored the portion of the Mori specification that explicitly teaches a process of forming a floating gate by patterning with a mask and etching. Anybody skilled in the semiconductor fabrication art knows that if a mask is used to form the floating gate, there is no way that the material of the floating gate can be limited to not extend beyond the edges of the trench, and if that were attempted, it would violate the design rules resulting in numerous alignment errors which in turn would result in extremely low yields of operative devices.

The Federal Circuit has clearly stated that even if a term has a meaning to an artisan which is different than the meaning assigned the term in the applicant's specification and prosecution history, the meaning given in the patent documents controls over any contrary or different meanings for the term commonly understood in the art. Southwall Technologies Inc. v. Cardinal IG Company, 34 USPQ2d 1673 (Fed. Cir. 1995).

The Examiner also rejected all the claims for obviousness over Mori standing alone. Why this happened is unclear, because if the Examiners rejected the claims for anticipation over Mori, why would they also reject them for obviousness unless they

were not exactly sure what the claims meant or what Mori teaches. The Examiner's 102 rejection of claim 2 (which also contains the self aligned limitation) is clear evidence that the Examiner has misinterpreted the self aligned limitation. Such a misinterpretation of a claim that condenses or modifies a critical claim limitation is fatal to the prima facie case of obviousness. ACS Hosp. Sys, Inc. v. Montefiore Hosp., 221 USPQ2d 929, 933 (Fed. Cir. 1985). In ACS, the invention was a television system for rental use including a key locked switch to turn the television on and off and an override switching means which, when activated, functioned to override the key locked switch even if it was off. The prior art primary reference (belonging to ACS) has no lockable key switch. The secondary references had no switching to overrided the keyswitch, only switching to override in general.

The district court held the claims obvious by generalizing the claim and determining that overriding of switches by providing an alternative current path to actuate an appliance is a commonly practiced technique. This holding was reached on grounds of the teaching of the primary reference, the ACS prior art and widespread use of override switches outside of TV rental systems.

The Federal Circuit reversed criticising the district court's claim construction as too generalized and finding that the district court's failure to find differences between the claimed invention and the prior art was clearly erroneous. The Federal Circuit noted that not a single reference addressed override switches in the TV rental industry and noted that the district court ignored this difference. Moreover, the Federal Circuit noted that the district court's application of the prior art ACS fully automated system to the claimed invention indicated a lack of attention to the explicit scope of the claimed switching elements.

In the Federal Circuit's view, the function of the switching element in the claimed invention was not similar to that of the automated ACS system which had no locked key switch. Specifically, the claimed invention had an override means to override the key locked switch, whereas the prior art ACS fully automated system used one switch to actuate the television and initiate billing. The reversal was based upon the district court's improper generalization of the claim.

Here, both Examiner's have erroneously generalized the claimed invention and

have misinterpreted the "self aligned" limitation as a process limitation. A self aligned floating gate clearly defines a structure not a process. As should be clear from the specification, a self aligned floating gate in a vertically oriented oriented EEPROM cell has no horizontal components or components orthogonal to the axis of the well. This means there is never any floating gate poly on the bottom of the well and never any floating gate poly on the top of the substrate around the perimeter of the well. The lack of floating gate poly on the top surface of the substrate means that all the structures around the well or trench are smaller since they only need to be aligned to the trench and not to any edges of the floating gate poly up on top of the substrate as is the case for the Mori cell.

Neither of them has fully comprehended nor given the self aligned floating gate limitation its true and specific meaning. This meaning can be easily determined from reading the specification and examining the drawings and process flow table in light of the knowledge of those skilled in the art. People skilled in the art know that integrated semiconductor devices are laid out using design rules and that a vertically oriented EEPROM memory cell with a self aligned floating gate (made without using a mask) will result in a smaller cell size than a vertically aligned EEPROM cell made using a mask to define the limits of the floating gate poly. People skilled in the art also appreciate that, just as was the case for Godzilla, size does matter, and it matters a great deal. In fact, size is everything in memory cell arrays with regard to how much they cost. The biggest impediment to the widespread use of nonvolatile EEPROM memory arrays in today's world which is being overrun with handheld computing devices is the cost per megabyte. The Examiner's here have exhibited an erroneous lack of attention to detail both as to the true meaning of key limitation of the claims on appeal and as to the actual scope and content of the teachings of the primary reference.

Concerning the self alignment of the Vora cell floating gate, the Examiner's have taken the following position in the Final Rejection.

> "Concerning self alignment, it is noted that the limitation is a process limitation, as discussed above. **It could conceivably be possible to define a self-alignment procedure to form Mori's floating gate. Mori does not show or disclose portions of the gate**

extending beyond the w ll. Thus, it is maintained that Mori discloses all the structural lem nts of claim 1. The claim language does not require the floating gates to be completely contained in the well, or set forth cell size. Limitations in the specification cannot be read into the claims for the purpose of avoiding prior art.

Even if it was true that the Mori cell could be made with a self aligned floating gate without doing harm to the operability or characteristics of the resulting structure, the resulting structure would still fall short of the claimed combination. The claimed combination of the Vora cell includes a bit line which is formed by depositing a third layer of poly on the surface of the substrate as opposed to being formed as a diffusion **in** the substrate as is done in the Mori cell. This means that the Vora cell would still enjoy several structural advantages over the Mori cell even if the Mori cell could be made with a self aligned floating gate. First, because the Vora cell bit lines (labelled as poly 2 bit line in Figure 33 of the Vora patent application - element 122) are on the surface of the substrate, they do not need to be made wider than the trenches as is the case for the Mori cell (see Col. 8, Lines 53 et seq.). The reason the Mori cell bit lines need to be wider than the trenches is precisely because they are diffusions that are **in** the substrate where the trenches will be etched down through them, so if they are not wider than the trenches, the trenches will cut them into segments destroying the continuity thereof for current flow to the sense amplifier. Further, the bit line diffusions need to be made wider than the Vora bit lines by virtue of the alignment tolerances required by the design rules so that correct registration of the trench mask with the bit lines is possible.

By forming bit lines in the substrate, Mori is forced in his contactless array to make the bit lines wider than the trenches so as to have narrow conductive paths of bit line around each trench to maintain continuity. These narrow paths increase the resistance of the bit line and slow the Mori access time by raising the resistance R in the RC time constant comprised of the bit line resistance and parasitic shunt capacitance to other structures. In contrast, because the Vora cells are formed on the surface of the substrate and not in it, they may be made of doped poly covered with silicide or metal and

can have much lower resistance than the Mori bit lines. This leads to faster access times for the Vora cell.

Further, by inspection of Figure 33 of the Vora patent application, it can be seen that the bit lines (122 in Figure 28B) are formed on the surface of the substrate by depositing doped polysilicon or metal over the word lines (110 in Figure 28B). The word lines are completely insulated on the top (by oxide 113 - see Fig. 28B) and on the sidewalls (by oxide spacers 114 - see Fig. 28B). Contact holes to expose the drain regions 86 at each EEPROM cell have been previously formed. The contact holes are self aligned to the edges of the spacer oxide layers 114 by the process explained at page 11, line 19 of the Vora specification with reference to Figures 27A, B and C. Basically, the contact holes are formed by using a mask to define photoresist over the adjacent CMOS devices outside the EEPROM array and to define the outer edges of the contact holes. The inner edges of the contact holes are self aligned with the spacer oxide 114 when the contact holes are etched through ONO layer 104 and oxide layer 84. Thus, when the bit line poly (third poly) or metal is deposited, it covers the tops of the word lines and is deposited into contact holes 118 and 120 in self aligned fashion to make contact with the drain regions 86. This forms a self aligned bit line which further reduces the size of the Vora cell. The cross sectional area of this bit line is never narrowed at the locations of the cells, so no increased resistance portions of the bit line are found in the Vora cell as are found in the Mori cell.

Thus, even if the Mori cell process were modified to self align the floating gate, the resulting structure would fall short of the claimed invention in that there would be no bit lines on the surface of the substrate since Mori's contactless array teaches buried bit lines formed in the substrate.

Further, with regard to the Examiner's statement that Mori could be self aligned and teaches all the elements of the claimed invention, there are several other errors of understanding of both fact and law. First, Mori does not teach a bit line which is formed on the surface of the substrate as called for by the claims. Second, a self aligned gate is a structure having specific physical characteristics which have been defined above. "Self aligned" is an adjective which defines floating gate and gives to it the structural characteristics defined in the specification. The Examiners stated one cannot read

limitations into a claim from the specification to avoid the prior art. While that is true, it is also evidences a misunderstanding by both Examiner's of the actual situation here and the holding of the Federal Circuit on this issue. First, to properly interpret the meaning of "self aligned floating gate" is not reading limitations into the claim from the specification. The limitation is already there and it is simply being interpreted in accordance with the specification, which is perfectly acceptable. The Federal Circuit noted this important distinction in Phonometrics Inc. v. Northeren Telecom Inc., 45 USPQ2d 1421, 1427 (Fed. Cir. 1998). There, the issue was claim construction of a phrase "call cost register means" with one party arguing that it had the meaning which could be gleaned from the specification that it was a structure which gave a caller a continuous readout of the running cost of the call during the call. The other party (the patentee) argued that the claim clause should be interpreted only as a structure which reflected the total cost of the call after the call has been terminated. the Federal Circuit held that the specification did not support the patentee's interpretation of its own claim since the specification was consistent throughout in explaining that the call cost register means had two functions of continuously reminding the caller as to the cost of the call as the call progresses and to indicate the total cost of the call after the call was completed.

Of significance here is the fact that the patentee argued that it was error to import additional limitations about continuous indication of call costs into the claim. The Federal Circuit rejected this argument stating:

> Phonometrics of course argues that additional limitations cannot be imported into a claim from the written description. We may, however, construe a specifically claimed limitation in light of the specification, which is all we do here.

That is all the applicant is asking the Board to do here - just properly construe an already present limitation to mean the structure described in the specification for the floating gate gate. Likewise, the Board should construe the rest of the structures in the cell that surround the well and the floating gate contained therein as having the relationships to the well that the claim calls for and that persons skilled in the art would understand for them in accordance with standard design rules rules that are known by every artisan in the semiconductor fabrication art.

Next, the Examiners note that it is "conceivably possible to define a self-alignment procedure to form Mori's floating gate". The Examiners are apparently saying that it would have been obvious to modify the teachings of Mori by changing the process to make the floating gate self aligned.

With regard to this position, an Examiner is not allowed to speculate on how a reference might be modified and without giving a specific explanation of the proposed modification and pointing out the evidentiary basis as to why the modification is supported by suggestion in the prior art. There must be evidence as to why a motivation to modify the primary reference or combine its teachings with teachings from secondary references before an obviousness rejection based upon such a modification or combination is valid. In re Jones, 958 F.2d 347, 351, 21 USPQ2d 1941, 1944 (Fed. Cir. 1992). There the Federal Circuit said:

> Before the PTO may combine the disclosures of two or more prior art references in order to establish prima facie obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988). We see no such suggestion in Zorayan, which is directed to shampoo additives, nor in Wideman, which teaches that the amine used to make the claimed compound is a byproduct of the production of morpholine. Nor does the broad disclosure of Richter fill the gap, for the reasons discussed above.
>
> Conspicuously missing from this record is any evidence , other than the PTO's speculation (if it be called evidence) that one of ordinary skill in the herbicidal art would have been motivated to make the modifications of the prior art salts necessary to arrive at the claimed 2-(2 '-aminoethoxy) ethanol salt. See Grabiak, 769 F.2d at 731-32, 226 USPQ at 872 ("[I]n the case before us there must be adequate support in the prior art for the [prior art] ester/ [claimed] thioester change in structure, in order to complete the PTO's prima facie case and shift the burden of going forward to the applicant."): In re Lalu, 747

> F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984) ("The prior art must provide one of ordinary skill in the art the motivation to make the proposed molecular modifications needed to arrive at the claimed compound.")

Neither Examiner has addressed the practical difficulties of whether or not the proposed modification of Mori can be done or whether the modified process would even work to create operable devices. In In re Newell, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989), the Federal Circuit held that the Board had erred in holding claims to a belt-to-capstan drive obvious over the capstan-to-capstan prior art. The Federal Circuit reversed and held the claims not obvious because the Board had not taken into account the practical difficulties in making the proposed modification or the properties the final structure made by the proposed combination or modification would have had. The Federal Circuit noted that it is part of the obviousness inquiry in determining whether suggestion or motivation does or does not exist to consider the problem the inventor solved (how to make a more compact EEPROM cell) and the properties the structure created by the proposed modification of the prior art or combination of prior art teaching would have. Specifically, the Federal Circuit held:

> The motivation to make a specific structure "is not abstract, but practical, and is always related to the properties or uses one skilled in the art would expect the [structure] to have, if made." In re Gyurik, 596 F.2d 1012, 1018, 201 USPQ 552, 557 (CCPA 1979). See also Fromson v. Advance Offset Plate, 755 F.2d 1549, 1556, 225 USPQ 26, 31 (Fed. Cir. 1985) ("The critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'") (Emphasis in original).
>
> In In re Wright, 848 F.2d 1216, 6 USPQ2d 1959 (Fed. Cir. 1988), we discussed the need, in comparing the differences between the structure and properties taught in the prior art, and those of the applicant's invention, to include consideration of the problem solved by the inventor. "The determination of whether a novel structure is or is not 'obvious' *requires cognizance of the properties of that structure* and the

problem which it solves, viewed in light of the teachings of the prior art." Id. at 1219, 6 USPQ2d at 1961-62. See In re Rothermel, 276 F.2d 393, 397, 125 USPQ 328, 332 (CCPA 1960):

> Where the invention for which a patent is sought solves a problem which persisted in the art, we must look to the problem as well as to its solution if we are to properly appraise what was done and to evaluate it against what would be obvious to one having the ordinary skills of the art.

Here, the Examiners have not addressed the practical difficulties of modifying the Mori process to make a self aligned floating gate nor suggested exactly how to do it. Further, the Examiner's have not explored the possibility that any anisotropic etch of the floating gate poly used in the Mori cell to make a self aligned floating gate might damage some other previously formed structures. Whether or not such previously formed structures would be damaged or the final structure made by the modified process would work is not at all obvious given the complexity of semiconductor processing and the lack of exact detail of the Mori process provided by the Mori reference.

Next, the Examiners state "it is maintained that Mori discloses all the structural elements of claim 1". This is not true. Claim 1 calls for a

> well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well

Mori does not teach a floating gate which is self aligned to not extend laterally beyond the edges of said well. Mori teaches at Col. 9, lines 23 et seq. how he forms his floating gate, to wit:

> The poly 1 deposition forms a conductive layer within each trench, including a vertically extending section 82. The vertically extending section 82 [c]overs the gate oxide 74 on the sidewalls of the trench, leaving a central cavity 84 in the trench.
>
> **The poly 1 layer is then patterned and etched to define floating gates.**

This combined with the showing of photoresist on top of the first poly layer 80 in Figure 4b is a clear teaching that a mask and photoresist are used to define the outline of the

floating gates for the etch. This mask must be aligned to the trench walls and the design rules will require minimum spacing between the walls of the trench and the edges of the floating gate poly to prevent registration errors from ruining the device. Thus, those skilled in the art will appreciate that it is absolutely impossible for the Mori device to have the poly of the floating gate completely contained within the walls of the trench area as claimed in claim 1. Some poly of the floating gate will alway lie on top of the substrate surrounding each trench in the Mori cell because the design rules require it to obtain adequate numbers of operative devices. The fact that the patent drawings seem to have the edge of the floating gate poly aligned with the edge of the trench. This is not controlling because the process clearly calls for a mask, and those skilled in the art know it would be impossible for the edges of the poly of the floating gate to actually be aligned with the edges of the trench.

Thus, Mori does not disclose every limitation in claim 1, and the Examiner's have erred in creatively reading nonexistent technical teachings into the Mori reference. Nothing in Mori can be interpreted as giving any significance to the fact that the drawings inaccurately show the edges of the floating gate poly aligned with the edges of the trenches, a fact which is inconsistent with the specific teachings of the specification and the way in which those teachings would be interpreted by those skilled in the art. Where an Examiner or the Board has misinterpreted the technical content of a prior art reference or read nonexistent technical description into it, the Federal Circuit has concluded that the burden to rebut a rejection for obviousness does not arise because the prima facie case of obviousness is not established. In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993).

There is no suggestion anywhere in the Mori reference of how the floating gate could be formed without a mask or of the desirability of building the cell in this way. The only suggestion of a way to make the cell smaller in the Mori reference is at Col. 1, lines 49 et seq. where it is suggested that the array can be made smaller by making the array contactless. In the Mori contactless array, no contact to the drain is made at every cell. Instead, the current from a cell being read must flow through the buried bit line all the way to the end of the row to a contact window and from there via a metal or other conductor on the surface of the substrate to the sense amp. This increases the resistance

of the Mori path for current from a cell being read to the sense amplifier which slows the access time. Mori recognizes this problem at Col. 1, line 52 where he notes contactless arrays have greater access time. This problem is exacerbated in Mori by the fact that the bit lines have reduced width portions at every trench thereby increasing the resistance ever further. The Vora cell does not have this problem since the bit lines are formed on top of the substrate and can be made of lower resistance poly by adding silicide (this is not possible in the Mori buried bit line for techical reasons those skilled in the art understand).

Where the prior art reference to be modified in support of an obviousness rejection does not even recognize the problem solved by the critical claim limitation, the Federal Circuit has noted that no motivation or suggestion to make a modification to solve this problem can be gleaned from such a reference. In re Nomiya, 509 F.2d 567, 184 USPQ 607 (CCPA 1975). In Nomiya, the problem solved by the invention was prevention of parasitic transistor action in IGFETs used in capacitive memory circuits. When IGFETS having protective diodes formed in the same substrate are used as switches to store data, a parasitic transistor action can take place causing discharge of the stored charge embodying the stored information thereby losing the stored information. The claimed solution was a voltage limiting means auxiliary to the protective diode which could be yet another protective diode formed outside the substrate or electrically isolated from the other circuit elements on the substrate. The Federal Circuit held that this claimed solution was not obvious because there was no evidentiary basis for the finding that a person of ordinary skill in the art would have had reason to apply an additional protective diode to a circuit that already had a protective diode given the fact that the reference did not even recognize the problem of the parasitic transistor action in the first place.

Here, the same rationale applies. The Mori cell already has a floating gate, and there is no recogniztion in Mori, that the cell could be made smaller by making the floating gate self aligned nor any suggestion of exactly how to do it. Given that state of affairs, a person of skill in the art would not perceive any suggestion to modify Mori to make it with a self aligned gate nor would there be any reason to perceive a reasonable liklihood of success in achieving an operative device by making the floating gate self

aligned since there is absolutely no guidance on how to make such a self aligned floating gate in Mori.

Since the properly interpreted self aligned floating gate claim limitation is not met exactly by the Mori reference, the anticipation rejection must fall. Since the self aligned floating gate limitation is not suggested by Mori and the problem it solves is not recognized by Mori, there is no suggestion to modify Mori to make it with a self aligned floating gate. Since the claims were all misinterpreted by both Examiners, the prima facie case of obviousness has not yet been established properly, and the final rejection is improper and should be overturned by the Board.

The Examiner Has Misunderstood The Applicability of Mori's Teachings To This Self Aligned Floating Gate Limitations in the Claims

The Examiner Has Misunderstood the Technical Content of the Teachings of the Mori Reference

The Mori reference does not teach a self aligned floating gate because the Mori floating gate has a horizontal component at the bottom of the trench and horizontal components at the top of the well overlapping the gate oxide layer. These components result because Mori does not teach use of an etch back to remove all horizontal components of the floating gate material as is taught in the applicant's specification.

If Mori taught the same invention as the applicant, there would be no horizontal component of the Mori floating gate either at the bottom of the well or above the gate oxide.

Further, Mori specifically teaches that the floating gate is formed by depositing first poly and then masking and etching to define the floating gates in each trench. At Col. 9 in the section entitled "2.3. Gate Conductor Formation", at lines 23 through 29, Mori teaches:

> "The poly 1 deposition forms a conductive layer within each trench, including a vertically extending section 82. The vertically extending section 82 covers the gate oxide 74 on the sidewalls of the trench, leaving a central cavity 84 in the trench.
>
> The poly 1 layer is then patterned and etched to define the floating gates."

Those skilled in the art know that the process being referred to in the quoted passage is a process which uses a mask to define the limits of the floating gate and is not a self aligned process. Self aligned processes do not use masks, and that is why they are preferred over process steps using masks because in self aligned processed, there are no registration errors. Further, there does not need to be any extra space left between structures to accomodate registration errors in a self aligned process. See the discussion in the next section for the significance of the difference in structure which results from applicant's self aligned process in terms of advantages it creates.

The "Self Aligned" Limitation In the Claimed Structure Gives Rise To Several Advantages Over the Mori Prior Art

Denser Array With More Tightly Packed Cells

Whenever a mask is used, more chip area must be consumed because the mask can have alignment errors on registration and extra space must be left between the proposed boundaries of the structure to be formed with the mask and adjacent structures so that registration errors do not cause adjacent structures to be affected by the process step or steps involving the mask in ways not intended. These cushions that Mori would have had to leave in constructing his floating gates use up die area and reduce the density of the array as compared to the self aligned floating gate formation process of the Vora patent application at bar. The difference in array density caused by this structural difference as well as the structural differences to be described below regarding the lack of a buried bit line in the claimed invention at bar lead to dramatic differences in array density, as pointed out in the Rule 132 Declaration of Madhu Vora.

Lower Programming Voltage Because Less Parasitic Capacitance Between the Floating Gate and the Drain and the Floating Gate and the Source

The lack of a self aligned floating gate in Mori causes Mori's programming voltage to be higher. This is a bad thing in very dense EEPROM arrays because higher programming voltages require separate power supplies or more complicated step up circuitry to raise the voltage of the Vcc supply. Higher programming voltages also require thicker insulation layers everywhere the programming voltage goes on the chip so as to prevent punch through and destruction of the chip.

Mori's program voltage is higher than the programming voltage of the applicant's cell for the following reason. The lack of a self aligned floating gate in the Mori device causes horizontal components of floating gate material to exist at the bottom of the well and at the top of the well. The horizontal component at the bottom of the well gives rise to a parasitic capacitance from the floating gate to the source. The horizontal component at the top of the well gives rise to a parasitic capacitance between the floating gate and the drain. The two parasitic capacitances create an equivalent circuit which is like that shown in Figure 3 of applicant's drawings with the two parasitic capacitances connected in parallel to C1. The two additional parasitic capacitances in the Mori device add to the capacitance C1 and make it larger relative to the capacitance of C2. The programming voltage causes tunnelling to the floating gate which occurs when a program voltage of some voltage such as 15 volts is applied to line 47 and a lower voltage, say 8 volts, is applied to the source line 49 in Figure 3. C2 and C1 form a voltage divider between the voltage on line 47 and the voltage of the channel region.

To minimize the programming voltage required to cause tunnelling to the floating gate, it is desired to have C2 greater than C1 so that most of the voltage drop between line 47 and the channel region occurs across C1. Because Mori does not use a self aligned floating gate, his C1 is larger than the C1 of the Vora cell described in this patent application, because the Vora cell does not have the two additional parasitic capacitors that raise the capacitance of C1. Therefore, Vora's programming voltage will be lower than Mori's, and this is a significant property of the Vora cell which gives it a significant advantage over the prior art Mori cell along with its greater density.

The "on said substrate" and "over said surface" and "on the surface" Limitations Of Claims 1 And 3-5, Respectively, Defining The Location Of The Bit Line As Above The Surface Of The Substrate Have Not Been Given Proper Weight

The Examiner has also misinterpreted the claim limitations defining the structure and location of the bit lines in all the claims. Claim 1 requires that the bit line contact comprise

> "a layer of conductive material formed *on* said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed *in* said

substrate."

Earlier in claim 1, the location of the drain region relative to the top surface of the substrate was specified by the following limitation:

> "a vertical MOS transistor formed by alternating N-type and P-type doped layers *in* said substrate..."

The intended and correct meaning for these limitations in light of the specficiation and drawings is a bit line which is *formed completely on top of the substrate which makes contact with the drain region formed in the substrate of the vertical MOS device at every cell.* This is what the drawings of this patent application show for the only embodiments disclosed and this is what the specification describes for the Vora cell. There is no broadening language in the specification that indicates the bit line may also be buried or formed in the substrate. The prior art references of record all show buried bit lines.

The Examiner has rejected claims 1 and 3-5 as being anticipated or obvious from the contactless array structure of Mori shown in Figures 1a and 1b.

The Examiner has misconstrued the Mori reference's teachings of a contactless array in stating:

> "A bit line contact 34a comprising a layer of conductive material in contact to drain layer 34 is assumed inherent to Mori's disclosure, as Mori shows an opening in insulating layer GO for said contact (Col. 5, lines 35-37, and Figure 1a), and such contact is necessary for the proper functioning of the device. *Thus, Mori discloses all the structural elements of claim 1.* (Emphasis mine)

The Examiner's conclusion that all structural elements of claim 1 are shown in the Mori contactless structure of Figure 1a is incorrect. First, Mori does not have a self aligned floating gate. Second, Mori's contactless array of Figure 1a does not have a bit line which is formed above the top surface of the substrate and which makes contact at every vertical MOS transistor location in the array, as called for by all of claims 1 and 3-5.

The Mori contactless array shown in Figure 1a teaches a buried bit line 34 to which electrical contact is made only at the end of the row at the location of contact window 34a. To a skilled artisan, this means that there is no bit line running along the

whole row above the surface of the substrate and making contact with the drain of each vertical MOS transistor in the row. The reasons an artisan would draw this conclusion (which is different than the Examiner's conclusion) from the Mori specification and drawings are as follows.

First, Mori specifically states at Col, 4, lines 48-50 that vertically stacked buried drain bitlines are used in the contactless array. With a buried bit line, there is no need for a bit line formed on the surface. There does need to be contact with the buried bit line, and that is the purpose of the contact window 34a through the GO gate oxide layer at the end of the row. But the presence of this contact window does not mean that there is a bit line on the surface that runs the length of the row and makes contact with the drain of every vertical transistor in the row as is the case for the Vora cell.

The price one pays for a buried bit line is higher resistance and slower access time. A bit line formed on the surface is exposed and can be metal or can be made of polysilicon with silicide deposited on top thereof. Both of these options are lower resistance than a buried doped bit line. Neither metal nor silicide can be used to lower the resistance of a buried bit line. Lower resistance for the bit line means a lower RC time constant in charging up all the parasitic capacitances coupled to the bit line in order to swing its voltage level enough to cause the sense amplifier to sense a change of voltage level. This means the voltage on the low resistance bit line on the surface of the substrate of the Vora cell can be changed more rapidly to cause an effect in the sense amplifier than is the case for a higher resistance buried bit line of the Mori cell and other references of record such as the Wong reference. This translates to shorter access time for the surface bit line structure than for the buried bit line structure.

Besides the fact that a buried bit line cannot be covered with silicide nor made of metal, there is the additional fact that the buried bit line of Mori will have periodic restrictions in the cross-sectional area through which current flows at the site of each trench. The reason for this is the buried bit line must act as a drain region at each trench but also must provide a continuous conductive path from each drain to the next. Thus, the bit lines must be slightly wider than the trench at the location of each trench so that the trench does not cut the conductive path completely off. Mori teaches this at Col. 8, lines 53-57 where Mori teaches that the width of the trenches must be selected

to be narrower than the width of the source and drain bit lines so that the source and drain bitlines provide a continuous conductive path along the respective row around the trenches. This means that narrow "runners" of conductive material of the drain bit line will run along the sides of each trench.

These narrow runners act as choke points for the current and raise the overall resistance of the bit line. The formula for the resistance of a conductive layer in an integrated circuit is:

$$R = \rho_s * \frac{L}{W}$$

where R is the resistance of the path;

ρ_s = the sheet resistance of the conductive material in ohms per square; and

L = the length of the conductor and

W = the width of the conductor.

Artisans recognize that the narrow runners increase the resistance. In fact, if the narrow runners each had a resistance of 400 to 800 ohms where the resistance of the bit line segments between the trenchs was 20 ohms, and there were 1000 cells in each row, the bit line resistance across the total row would be in the megohms, and the array would be inoperative as an EEPROM memory.

Thus, Mori's contactless array cell, nor any of the other references of record, teach all the claimed elements, as properly interpreted, combined in the same way as are found in the rejected claims so the anticipation and obviousness rejections of claims 1 and 3-5 are respectfully requested to be withdrawn.

A Bit Line On The Surface Of A Substrate Need Not Be Wider Than The Trench And Can Lead To A Denser Array

There is another advantage in putting a bit line on the surface of the substrate. That advantage is that the bit line need not be formed to be wider than the trenches as in Mori. This can lead to greater array density because of less spacing between rows since no space between rows is taken up by the runners and suitable safety margins to prevent registration errors from rendering the chip inoperative.

Self Aligned Is Not A Process Limitation

The Examiner took the position that the modifier self aligned for the floating gate limitation is a process limitation. This is not true, and the undersigned respectfully request reconsideration of this position. A self aligned gate in the planar MOS transistor world has definite structural meanin in that the drain and source region edges will be precisely aligned with the edges of the oxide spacers at the edges of the gate.

Likewise, a self aligned floating gate in a vertical transistor now has structural meaning in that the modifier defines a gate with vertical components on the walls of the well only with no horizontal components at the bottom of the well or over the top surface of the substrate such that the bit lines can be made more narrow and the cells may be spaced closer together.

Further, because the Mori floating gate is formed with a mask, there is a distinct possibility that the edges of the floating gate will extend beyond the edge of the well depending upon the mask configuration and any registration errors with the mask that defined the trench location and size.

The Structure Of The Examiner's Obviousness Rejection Is Improper

The Examiner stated that it would have been obvious to modify the Mori reference to add:

> "a bit line contact to the transistor drain extending into opening 34a disclosed by Mori. The rationale is as follows: one of ordinary skill in the art at the time the invention was made would have been motivated to do so as such bit line contact was necessary for operation of the memory cell."

This does not provide a proper showing of evidence of motivation or suggestion to modify the primary reference. Motivation or suggestion is supported by something in the prior art references or the general level of skill that suggests a particular combination of elements from two or more references or a particular modification of a primary reference along the lines of the invention claimed would have a reasonable liklihood of success in solving the problem solved by the invention. In re Newell, 13 USPQ2d 1248, 1250 (Fed. Cir. 1989) ["The motivation to make a specific structure is not abstract, but practical, and is always related to the properties or uses one skilled in the art would expect the structure to have, if made."]; In re Gurley, 31 USPQ2d 1130, 1131 (Fed.

Cir. 1994) [a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. In general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant.]

Here, there was no motivation provided by the prior art to modify the Mori contactless array of Figure 1a to provide a bit line totally above the surface. This is because the Mori contactless array of Figure 1a already has a buried bit line and does not need another one on the surface. The Mori reference does suggest a surface bit line embodiment in Figure 2b, but this suggetion does not include a self aligned floating gate, and is coupled with the suggestion at Col. 1, lines 50-52 that putting the bit line on the surface makes the array bigger. This is because Mori suggests in Figure 2b and its accompanying text that a contact window to the drain must be formed at each cell location and adjacent to the trench to make contact to the drain of every cell. This contact window will have to be spaced by the design rules away from the trench at every cell and will cause each cell to be larger and the overall array much less dense.

This is the opposite result from which Mr. Vora was trying to achieve - Mr. Vora invented a cell structure that can be both small and fast. The smallness comes from the self aligned floating gate, and the speed of access comes from the fact that the bit lines are completely on top of the substrate so they have so width restrictions and can be made of low resistance materials. Further, they make contact with the drain region at every cell so current from a cell being read does not have to make its way through a high resistance buried bit line all the way to the end of the row before surfacing and being conducted by a low resistance path to the sense amplifier.

The Examiner is not allowed to make bald conclusions of the existence of suggestion or motivation to make a combination or modification. The Examiner must be able to point to specific evidence in the prior art that supports his or her conclusion of the existence of suggestion or motivation. In re Jones, 21 USPQ2d 1941, 1944 (Fed. Cir. 1992).

Nor is there suggestion proven by the Examiner to modify the Mori reference to

make the floating gate self aligned as that term is used in the claims. The Examiner is not allowed to read nonexistent technical description into a reference and cannot read importance of a factor into a reference if the reference itself does not assign importance to the factor. In re Rijckaert, 28 USPQ2d 1955 (Fed. Cir. 1994). Here, there is no description of a self aligned floating gate in Mori nor is there a recognition of the problem of extra parasitic capacitance caused by the horizontal components. Mori also does not recognize the problems of degradation of array density by using a mask to define the extents of the floating gates and assigns no importance whatsoever to having no horizontal components of the floating gate. If the prior art fails to recognize the problem solved by the invention, an artisan would not be motivated by the reference to solve the unmentioned problem. In re Nomiya, 184 USPQ 607 (CCPA 1975).

The Declaration under 37 CFR 1.132 of Madhu Vora provides ample evidence to overcome the prima facie obviousness case if the prima facie obviousness case was ever actually established. We dispute that a prima facie case of either anticipation of obviousness was ever actually established because of the misinterpretation of critical claim limitations and misreading of the prior art. In his Rule 132 Declaration, Mr. Vora did a sample layout of the Mori cell and Vora cell using industry standard design rules for 1 micron and 0.35 microns. The Mori cell was laid out with the teachings of the Mori contactless cell from the patent. Mr. Vora concludes that the Vora cell on the average is about 3 times smaller than the Mori cell and the array for a 1 square centimeter die is approximately 3-4 times as dense. The principal reasons are the use of a self aligned gate in the Vora cell, and the lack of an isolation barrier and buried layer source implants. The Vora cell does not used buried layer source implants. Instead, the entire substrate has a doped N- layer that serves as the source which is grounded thereby eliminating the need for isolation barriers. The use of the self aligned gate is a large contributor to the small size of the Vora cell.

All claims are believed to be in condition for allowance, and favorable action is ernestly solicited.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed:Commissioner of Patents and Trademarks, Washington D.C. 20231 on (Date Of Deposit) August 4, 1998.
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APPENDIX - CLAIMS ON APPEAL

1. (Amended) A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by alternating N-type and P-type doped layers in said substrate [intersecting] and wherein a well is etched into said substrate through said alternating N-type and P-type layers such that said alternating layer surround said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well and insulated from and overlying said alternating N-type and P-type [materials] layers by a layer of gate insulating material;

a word line contact comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said [flaotign] floating gate but insulated therefrom by an insulation layer; and

a bit line contact comprising a layer of conductive material formed on said substrate so as to be in electrical contact with the drain region of said vertical MOS transistor formed in said substrate.

2. (Amended) A nonvolatile memory cell array comprised of a plurality of nonvolatile memory cells, each memory cell comprising:

a semiconductor substrate having a drain region of a first conductivity type formed therein and having a surface coincident suitable to act as a drain region of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel [region] of a vertical MOS transistor formed in said substrate;

a [first] source region of said semiconductor substrate [between said buried layer and said surface of said substrate, and a second region of said semiconductor substrate] below said channel region [buried layer, both said first and second regions] source region being doped so as to have [a] said first conductivity type;

[a first layer of insulating material covering said surface of said substrate;]

a recessed gate window in the form of a well etched in said semiconductor substrate

through said first layer of insulating material, said well being deep enough to penetrate through said [buried layer] channel region and into said source region such that at least some portion of the side wall or sidewalls of said trench are bordered by said source, drain and channel regions [recessed gate window intersect said buried layer and said first and second regions of said semiconductor substrate];

[a second] an insulating layer covering the bottom of said well;

a gate insulating layer formed on the sidewall of said well;

a self aligned floating gate comprising a conductive material formed within said well on said gate insulating layer so as to not extend beyond the edges of said well; [with]

an insulating layer formed over said self aligned floating gate [conductive material] so as to electrically isolate said floating gate from all surrounding structures, said floating gate having a dimension suitable so as to overlie at least said [intersection of said well with said buried layer] channel region;

a word line comprising conductive material deposited [on said first insulating layer] so as to extend into said well far enough to overlie at least a portion of said floating gate; and

a second layer of insulating material formed [over] so as to insulate at least a portion of said word line; and

a bit line formed over said surface of said semiconductor substrate so as to make contact with at least a portion of said drain region at each said memory cell but insulated from said word line by said second layer of insulating material[, and deposited in a contact window formed in said first insulating layer so as to be in electrical contact with said first region, said first region acting as a drain of said vertical MOS transitor].

Please add a new claim 3 as follows:

3. A nonvolatile memory cell array comprised of a plurality of EEPROM memory cells, each cell comprising:

a semiconductor substrate;

a vertical MOS transistor formed by a first layer of N-type conductivity and having a surface coincident with the surface of said substrate and forming a drain region of said vertical MOS transistor, a second layer of P-type conductivity within said substrate and adjacent to and underlying said first layer relative to the surface of said substrate and forming a channel region of said vertical MOS transistor, and a third layer of N-type conductivity within said substrate and adjacent to and underlying said second layer and

forming a source region of said vertical MOS transistor, and having a well etched into said substrate so as to penetrate through said first and second layers and at least partially through said third layer, said well having a floating gate of conductive material formed therein which is self aligned so as to not extend laterally beyond edges of said well and overlying said first, second and third layers and insulated by a layer of gate insulating material from said first, second and third layers;

a word line comprising a layer of conductive material formed on said substrate so as to extend down into said well and overlie said floating gate but insulated therefrom by an insulation layer;

a bit line comprising a layer of conductive material formed on the surface of said substrate so as to be in electrical contact with the surface of said first layer coincident with the surface of said substrate at each cell in said array, and

a spacer layer of insulating material insulating said word line contact from said bit line contact.

4. The apparatus of claim 3 wherein said bit line contact contacts said first layer at all points between said spacer layers of the word line contacts of adjacent memory cells.

5. The apparatus of claim 3 wherein said bit line contact contacts said first layer at at least some points between said spacer layers of the word line contacts of adjacent memory cells and runs over the top of said word line and is insulated therefrom by said spacer layer.

EXHIBIT 1

MORI CELL LAYOUT BY MADHU VORA 6/4/98

1 UM DESIGN RULES